Software in a Hardware Domain

Software for the CFT L1 Trigger

What is the Hardware

- FPLD - Field Programmable Logic Device
- FPLD - An FPGA plus other features
  - Field Programmable Gate Array
  - Embedded Array Blocks
  - Commercial logic cores

New Commercial Uses

- Co-processors
- embedded DSP's
- self configuring interface
  - self re-program depending on needed use
  - switch between program in few msec

L1 Trigger Problem

- Each Road of CFT is 1 Equation
  - Tr(i) = A(a) * B(b) * …. *H(h) -> 8 fold
- Each Sector (1/80th)
  - 44 Outer bins > h values
  - +- 16 Pt offsets > a values
  - 12 comb. Of B-G > b through G values
- Number of ‘Equations’
  - 44 * 12 * (2 * 16) = 17k (1.3M)

Time to Solve Problem

- With 333MHz serial processor
  - 3ns * (17,000/6) equations * N steps
  - (8.5 * N) us
- With FPLD (ALTERA 10K250)
  - 300 ns

How to Program

- VHDL - Virtual Hardware Design Language
- High level textual language
- Supports
  - sub-routine trees
  - local and global variables
  - simulations
- Language Standard (IEEE)

Example of Program

- Frame in terms of integers - don’t get stuck with bits
- Coded for Programmer - program for clarity to the programmer, maintenance of code
- Strong optimizers link general code to specific hardware, better than person can

Summary

- Major complexity of trigger is in FPLD coding
- Can code in High level language where the problem can be expressed in your terms
- Can develop code and simulate on desktop
- Hardware is more of a ‘Software’ world